

24th Year

1986-2010

ADVANCE PROGRAM

**2010 IEEE BIPOLAR / BiCMOS
CIRCUITS AND
TECHNOLOGY MEETING**

www.ieee-bctm.org

**Radisson Hotel & Suites
Austin, Texas, USA**

OCTOBER 5 – 6, 2010
SHORT COURSE — OCTOBER 4, 2010



SPONSORED BY

**THE ELECTRON DEVICES SOCIETY OF
THE INSTITUTE OF ELECTRICAL AND
ELECTRONIC ENGINEERS**

IN COOPERATION WITH

**THE IEEE SOLID-STATE CIRCUITS SOCIETY
THE IEEE MICROWAVE THEORY &
TECHNIQUES SOCIETY**



2010 BCTM SCHEDULE AT A GLANCE			
Monday — October 4 Registration open from 7:30 AM-5:00 PM MEZZANINE NEXT TO TRAVIS II			
7:30 AM — 5:30 PM	SHORT COURSE – TRAVIS III <i>Si/SiGe Circuit Design for Applications from GHz to THz</i>		
Tuesday — October 5 Registration open from 8:00 AM – 5:00 PM MEZZANINE NEXT TO TRAVIS II			
9:00 AM	Opening Remarks and Announcements		
9:15 AM — 10:00 AM	Keynote Speaker – Dr. Thomas Lee The Fourth Age of Wireless: The Last and Best? TRAVIS I, II, III		
10:00 AM	Coffee Break – Mezzanine		
10:25 AM — 12:30 PM	1. RF & mmWave VCOs TRAVIS I & II	2. High Bitrate Circuits TRAVIS III	3. BiCMOS, C-BiCMOS, C-Bipolar Technologies and Devices LAKEVIEW
12:30 PM	Lunch Break		
2:00 PM — 4:05 PM	4. mmWave Transceivers TRAVIS I & II	5. Integrated BiCMOS Components TRAVIS III	6. State-of-the- Art Modeling and Characterization LAKEVIEW
4:05 PM	Coffee Break – Mezzanine		
4:25 PM — 6:30 PM	7. 4G Radio Design and PAs TRAVIS I & II	8. Robustness and Thermal Limitations TRAVIS III	9. High-Frequency and Noise Modeling LAKEVIEW
7:00 PM — 11:00 PM	Dinner Banquet Poolside Texas BBQ		
Wednesday — October 6 Registration open from 8:00 AM – 10:00 AM MEZZANINE NEXT TO TRAVIS II			
8:00 AM — 10:15 AM	10. Emerging Technologies Session TRAVIS I, II, III		
10:15 AM	Coffee Break – Mezzanine		
10:35 AM — 12:15 PM	11. Mixers and LNAs TRAVIS I & II	12. New Device Concepts TRAVIS III	13. Analog Potpourri LAKEVIEW
12:15 PM — 1:30 PM	Luncheon and Luncheon Talk: “Advanced Avionics, the Constellation Program, and NASA’s Manned Spaceflight Future” <i>Dr. Andrew Keys, NASA</i> AUSTIN BALLROOM		
END OF MAIN BCTM CONFERENCE START OF CMRF SPECIAL SESSION			
1:30 PM — 3:30 PM	CMRF 1 Crossing the Boundaries of Modeling TRAVIS III		
3:30 PM	Coffee Break- Mezzanine		
3:45 PM — 5:00 PM	CMRF 2 Crossing the Boundaries of Modeling TRAVIS III	CMRF 3 Modeling of Thermal Effects TRAVIS I & II	
END OF CMRF SPECIAL SESSION			

Welcome from the BCTM 2010 Chairmen

On behalf of the Executive Committee, we would like to welcome you to the 2010 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM). The BCTM 2010 will be held 4th-6th October, 2010 at the Radisson Hotel & Suites Austin-Town Lake. It includes a one day short course and two days of the conference.

Anyone interested in leading edge processes, devices, and circuits used in state of the art telecommunication systems and power control systems will not want to miss this conference. Bipolar and BiCMOS technologies, particularly SiGe HBT BiCMOS technologies, continue to play a key role in these systems.

Papers covering the design, performance, fabrication, testing, modeling, and application of bipolar and BiCMOS integrated circuits, bipolar phenomena, and discrete bipolar devices will be presented.

Located in Central Texas on the eastern edge of the [American Southwest](#), Austin is the fourth-largest city in Texas and the 15th-largest in the United States. The city is home to development centers for many technology corporations and has adopted the nickname "Silicon Hills". Additionally, the city's official slogan promotes it as "The Live Music Capital of the World", a reference to the many musicians and live music venues within the area.

The conference starts with a one day short course followed by two full days of contributed and invited papers including keynote speaker and a special session on Emerging Technologies. On Tuesday evening, we will have our Gala Dinner, an annual highlight of the conference which offers attendees a great opportunity to catch up with old colleagues and make new friends.

The short course features three renowned experts on "Si/SiGe circuit design for applications from GHz to THz". Short course invited talks include: "Fully Integrated RF Front-Ends in SiGe BiCMOS", Peter Gammel (SiGe Semiconductors), "Development of Millimeter-wave Phased-arrays for Communication", Scott Reynolds (IBM), and "Design of Silicon Integrated THz Circuits", Ullrich Pfeiffer (University of Wuppertal).

We are fortunate to have Dr. Thomas Lee from Stanford University as this year's keynote speaker. Dr. Lee will discuss "The Fourth Age of Wireless: The Last and Best?" This is a great opportunity to meet Dr. Lee and learn about the latest trends in advanced communication technologies.

On Wednesday, our conference will feature two special sessions: Emerging Technologies and RF Compact Modeling. Three leading experts from the electronics community will share their visions during the special Emerging Technologies session. The first speaker is Professor Frank Schwierz from Technische Universitat Ilmenau, who will present "Graphene Applications and with Special Focus on the Graphene Transistors." Our next speaker, Dr. Christian Person of Lab-STICC Laboratory/Telecom Bretagne, will give some insights on "Silicon Antennas." And our Emerging Technologies session will be completed with "The Future of Medical Electronics" presented by Dr. Karthik Vansath, TI's Medical Business.

The compact modeling session will focus on two areas, "Crossing the Boundary of Modeling" and "Modeling Thermal Effects". A unique discussion of the interrelationship between the TCAD device level simulator and compact analytical device models will be explored in the first session, "Crossing the Boundary of Modeling". While there are a number of papers in the literature discussing compact analytical models or detailed device level simulations, there are few conference sessions that explore the interrelationship between the two. A parallel session, "Modeling of Thermal Effects", will take an in depth look at electro-thermal and thermal resistance modeling.

Two days of technical paper sessions, a luncheon with guest speaker Andrew Keys of NASA, and the evening banquet round out the program. We look forward to welcoming you at BCTM 2010. See you in Austin!



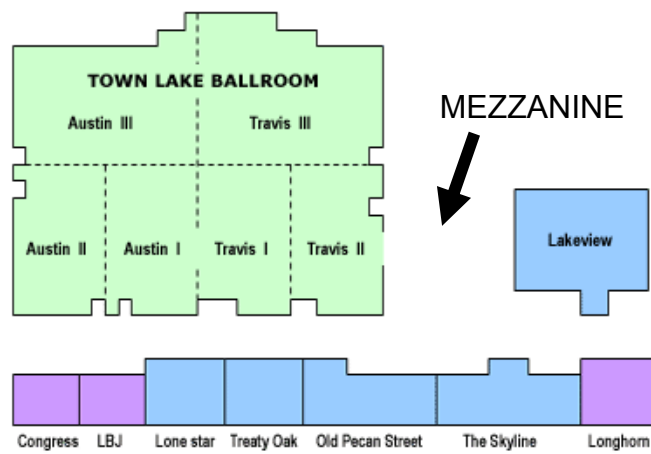
*David Ngo, RFMD
General Chairman*



*Alvin Joseph, IBM
Technical Program Chairman*

Radisson Hotel & Suites Austin-Town Lake

Conference & Meeting Room Layout



BCTM Short Course
Si/SiGe Circuit Design
for Applications from GHz to THz

Date: Monday, October 4, 2010
Time: 7:30 AM - 5:30 PM
Location: **TRAVIS III**

Course Overview

Already for many years Si/SiGe BiCMOS is the technology of choice for many high frequency applications. And the continuous development of faster transistors, more advanced processes, and improved circuit design techniques have further expanded the domain of silicon from the lower GHz range and low power to RF and millimeter-wave frequencies, power and front-end applications, phased-array systems, and even towards the THz range.

For this Short Course we have therefore invited three renowned experts to address the challenges, trade-offs, and performance for applications from GHz to THz. We recommend everyone interested in leading edge circuit design and technology to attend, and look forward to see you!

Fully Integrated RF Front Ends in SiGe BiCMOS

Instructor: Peter Gammel, SiGe Semiconductor

Fully integrated RF front ends, including linear and saturated power amplifiers, low noise amplifiers, RF switches, filters and associated analog circuitry for power detection and control can be achieved using 350nm SiGe BiCMOS technology. With the extension of BiCMOS technology to include through silicon vias and high resistivity substrates, linear power amplifiers for WLAN at 2GHz and 5GHz up to 26dBm at 3% EVM can be achieved, with all match fully integrated onto the die. Saturated power amplifiers at 900MHz and 2.5GHz for Zigbee applications are considered, with a focus on off state leakage to improve battery life. Transistor sizing and breakdown requirements are reviewed, and the impact of both emitter and base ballasting on amplifier performance, ruggedness and stability are explored. The proper design and shielding of inductors for input, interstage and output match is considered, and architectures to improve power amplifier efficiency will be briefly discussed.

Low noise amplifiers, both narrow band and broadband are achieved in SiGe bipolars, and the performance of passive filter and matching networks are reviewed. To complete the elements for RF front ends, the performance of CMOS RF switches are considered, as well as the complexities of integration of all RF functions on a single die, while meeting stringent regulatory requirements on harmonic and other spectral emissions.

Peter Gammel holds a PhD in physics from Cornell University and Bachelor of Science degrees in physics and mathematics from MIT. He currently is Chief Technical Officer and Vice President Engineering at SiGe Semiconductor, the leading fabless RF design company utilizing SiGe BiCMOS for WLAN, GPS and Zigbee RF front ends. Peter previously served as VP engineering at a venture-backed startup focused on tunable RF front ends. Prior to that, he was chief technology officer at Agere Systems (analog products business unit), and was research director at Bell Laboratories. His research career also included work on single-electron devices, superconducting

devices, and MEMS and RF acoustic wave devices spanning more than 25 years.

Development of Millimeter-Wave Phased-Arrays for Communication

Instructor: Scott K. Reynolds, IBM T. J. Watson Research Center

This presentation will begin with a brief review of phased-array and millimeter-wave principles, then describe the development of a 16-element phased-array transceiver chipset in 0.13- μm SiGe BiCMOS. These receiver and transmitter ICs have each been packaged with 16 antennas in low-cost multi-layer organic packages, using a 288-pin ball-grid array format. The ICs have been used in non-line-of-sight communications links at rates $> 5\text{Gb/s}$ in each of the frequency channels of the IEEE 802.15.3c standard (58.32 to 64.8 GHz).

The Rx and Tx ICs each use a double-conversion superheterodyne architecture with on-chip frequency synthesizer. The 16 RF front-ends of both Tx and Rx ICs incorporate balanced reflection-type phase shifters with digitally-controlled phase resolution of $11^\circ \pm 3^\circ$. The Tx delivers 9 to 13.5 dBm $\text{OP}_{1\text{dB}}$ per element at 60.48 GHz and features $\text{OP}_{1\text{dB}}$ programmability through the bias control of its final stage. The Rx has a maximum of 72 dB of power gain in 1-dB steps and achieves 7.4-7.9 dB NF (not including 12-dB array gain) over the 4 IEEE channels. Measurement results from packaged ICs in an antenna chamber are also discussed, including the demonstration of spatial power combining up to +40dBm EIRP and 16-element radiation patterns.

Scott K. Reynolds received a Ph.D. in electrical engineering from Stanford in 1987. He joined IBM in 1988 and has worked on a wide variety of IBM products, including ICs for disk drive channels, electrical and optical I/O, and RF communication. He has recently been engaged in development of silicon millimeter-wave ICs and packaging for high-data-rate wireless links and other applications. He has more than 25 U.S. patents and many technical publications, including two papers on 60-GHz wireless transceiver circuits which won the best paper awards at ISSCC in 2004 and 2006. He currently manages the RF Circuits & Systems group at the IBM T. J. Watson Research Center.

Design of Silicon Integrated THz Circuits

Instructor: Ullrich Pfeiffer, High-Frequency and Communication Technology (IHCT), University of Wuppertal, Germany

Applications such as imaging, spectroscopy, chemical/biologic identification, hidden object detection, and communication with ultra-high data-rates have increased the interest in silicon-based THz detection systems. The push in frequency imposes a number of challenges for the design of THz circuits in silicon process technologies. The short course will describe recent attempts to mitigate power and sensitivity limitations based on SiGe and CMOS process technologies. In particular, the course will describe sub-harmonic and distributed resistive mixing techniques to operate silicon transistors above their cut-off frequency.

The techniques will be explained with the help of practical circuit design examples from 160 to 650 GHz. Among others, this includes monolithically integrated 0.65 THz CMOS focal-plane arrays, 0.65 THz sub-harmonically pumped SiGe HBT imaging front-ends including integrated antennas, and a 158-165 GHz TX and RX chipset

supporting QAM modulation schemes in SiGe. Finally, raster-scanned imaging examples will demonstrate the potential of silicon for future THz imaging applications.

Ullrich R. Pfeiffer received the diploma degree in physics and the Ph.D. in physics from the University of Heidelberg, Germany, in 1996 and 1999 respectively. From 2001 to 2006 he was with the IBM T.J. Watson Research Center where his research involved RF circuit design, power amplifier design at 60GHz and 77GHz, high-frequency modeling and packaging for millimeter-wave communication systems. Since 2008 he holds the High-frequency and Communication Technology chair at the University of Wuppertal, Germany. His current research activities include the design of silicon integrated circuits for THz imaging applications.

BCTM Short Course Schedule**Si/SiGe Circuit Design
for Applications from GHz to THz**

Date: Monday, October 4, 2010

Time: 7:30 AM - 5:30 PM

Location: **TRAVIS III**

7:30 – 8:30 Short Course Registration (Mezzanine)

7:30 – 8:30 Continental Breakfast

for Short Course Attendees (Mezzanine)

8:30 - 8:45 Welcome:

Léon van den Oever and Hugo Veenstra

8:45 - 9:45 **Fully Integrated RF Front Ends in SiGe
BiCMOS**

Dr. Peter Gammel, SiGe Semiconductor

9:45- 9:55 Break

9:55-10:55 **Fully Integrated RF Front Ends in SiGe
BiCMOS (continued)**

10:55-11:25 Break

11:25-12:25 **Development of Millimeter-Wave
Phased-Arrays for Communication**

Dr. Scott K. Reynolds,

IBM T.J. Watson Research Center

12:25 - 1:50 Short Course Lunch – **TRAVIS I & II**

1:50 - 2:50 **Development of Millimeter-Wave
Phased-Arrays for Communication
(continued)**

2:50 - 3:00 Break

3:00 - 4:00 **Design of Silicon Integrated THz Circuits**

Prof. Ullrich Pfeiffer,

High-Frequency and Communication

Technology (IHCT), University of Wuppertal

4:00 - 4:30 Break

4:30 - 5:30 **Design of Silicon Integrated THz Circuits
(continued)**

5:30 Close with Short Course Evaluation

GENERAL INFORMATION

ADMISSION All interested persons are welcome to register and attend the BCTM; you do not have to be an IEEE member. Admission to sessions requires a BCTM badge. Please wear your badge at all times.

REGISTRATION Complete registration information is contained in the centerfold of this booklet as well as on the conference's web page (www.ieee-bctm.org). Please use the website to register. The advance registration deadline is September 17, 2010. All conference activities are included in the registration fees (technical sessions, luncheon, and banquet) as well as a CDROM and printed copy of BCTM 2010 Proceedings. The 2010 Special Session on Compact Models for RF-Microwave Applications (CMRF) is also included for BCTM attendees. Additional copies of BCTM 2010 Proceedings can be obtained. Details are shown in the registration centerfold of this booklet.

DINNER BANQUET The dinner banquet takes place on October 5, 2010, Tuesday evening, at the Radisson Hotel & Suites.

OTHER CONFERENCE SOCIAL EVENTS Several events have been arranged to promote informal social interactions between conference participants.

LOCATION The 2010 BCTM is located in Austin, Texas:
Radisson Hotel & Suites, Austin-Town Lake,
111 Cesar Chavez at Congress, Austin Texas 78701, USA.

SURROUNDING AREA Located in Central Texas on the eastern edge of the American Southwest, Austin is the fourth-largest city in Texas and the 15th-largest in the United States. It was the third-fastest-growing large city in the nation from 2000 to 2006. Residents of Austin are known as "Austinites" and include a diverse mix of university professors, students, politicians, musicians, state employees, high-tech workers, blue-collar workers, and white-collar workers. The main campus of the University of Texas is located in Austin. The city is home to development centers for many technology corporations and has adopted the nickname "Silicon Hills". Additionally, the city's official slogan promotes it as "The Live Music Capital of the World", a reference to the many musicians and live music venues within the area.

TUTORIAL / SURVEY TALKS Tutorial talks given by invited experts are intended to give a broad overview of a given subject with a critical review of technology and applications. They are twice the length of the usual contributed talk with longer abstracts in the Proceedings.

AIRLINES & LOCAL TRANSPORTATION The closest airport is the Austin-Bergstrom International Airport, which has direct connections with most major US cities and airline hubs. Detailed travel information can be found at the BCTM 2010 website (<http://www.ieee-bctm.org>) or the Austin Airport webpage : <http://www.ci.austin.tx.us/austinairport/>

HOTEL ACCOMMODATIONS The Radisson Hotel & Suites at Austin-Town Lake has a room block available for conference attendees. Please make your reservations early to benefit from the conference rate. Attendees can contact the Hotel directly to make their reservations, as indicated in the BCTM 2010 website (<http://www.ieee-bctm.org>). When making reservations by phone, be sure to inform the hotel that you are with the IEEE BCTM. Further information for accommodation in Austin can be found in the BCTM 2010 website.

MEMBERS OF THE PRESS The press is welcome at the BCTM and is offered FREE admission. Just present your business card at the registration desk.

FUTURE MEETINGS BCTM 2011 will be held in Atlanta, Georgia, USA. Alvin Joseph is the BCTM 2011 Conference Chairman (josepha@us.ibm.com). A description of the conference sites and details will be posted at: www.ieee-bctm.org.

RECRUITING Intensive recruiting undermines the purposes for which the BCTM was established, and is contrary to IEEE policy.

BEST STUDENT PAPER AWARD BCTM presents an award for Outstanding Student Paper. To be considered for the award the student must be the lead author and speaker at the conference. The award consists of an engraved plaque and \$500, and is based on the technical quality of the published manuscript, clarity of the oral presentation, and the evaluation of the Technical Program Committee.

FURTHER INFORMATION BCTM is sponsored by the IEEE Electron Devices Society (EDS) in co-operation with the IEEE Solid-State Circuits Society (SSCS) and the IEEE Microwave Theory & Techniques Society (MTT).

Tuesday, October 5, 2010

WELCOME AND OPENING REMARKS

9:00–10:00 AM — **TRAVIS BALLROOM, I, II, III**KEYNOTE SPEECH**The Fourth Age of Wireless: The Last and Best?***Dr. Thomas H. Lee, Stanford University*

Although predicting the future is an inherently foolish endeavor, the lessons of history can perhaps provide us with outlines of probable futures.

Wireless -- now in its third age -- is a runaway success by any measure. Two-thirds of the developed world is already connected wirelessly, and more than three million handsets are sold daily. This success is the latest stage in a process of punctuated evolution, which began with Marconi's station-to-station wireless telegraphy. Station-to-people broadcasting followed, and peacefully coexists for the moment with today's people-to-people cellular. Each transition between ages surprised the incumbent, and each transition saw a dramatic increase in value by dramatically increasing the number of conversants. Having already covered all possible combinations of "stations" and "things," one might argue that the history of wireless is essentially complete. This talk describes a coming Fourth Age of wireless, which accommodates communication with (and between) objects. The wireless "internet of everything" will represent a "completion" of history, the last and the best age of wireless.

Thomas H. Lee received the S.B., S.M. and Sc.D. degrees in electrical engineering, all from the Massachusetts Institute of Technology in 1983, 1985, and 1990, respectively.

He joined Analog Devices in 1990 where he was primarily engaged in the design of high-speed clock recovery devices. In 1992, he joined Rambus Inc. in Mountain View, CA where he developed high-speed analog circuitry for 500 megabyte/s CMOS DRAMs.

He has also contributed to the development of PLLs in the StrongARM, Alpha and AMD K6/K7/K8 microprocessors. Since 1994, he has been a Professor of Electrical Engineering at Stanford University where his research focus has been on gigahertz-speed wireline and wireless integrated circuits built in conventional silicon technologies, particularly CMOS.

He has twice received the "Best Paper" award at the International Solid-State Circuits Conference, co-authored a "Best Student Paper" at ISSCC, was awarded the Best Paper prize at CICC, and is a Packard Foundation Fellowship recipient.

He is an IEEE Distinguished Lecturer of the Solid-State Circuits Society, and has been a DL of the IEEE Microwave Society as well. He holds 43 U.S. patents and authored *The Design of CMOS Radio-Frequency Integrated Circuits* (now in its second edition), and *Planar Microwave Engineering*, both with Cambridge University Press. He is a co-author of four additional books on RF circuit design, and also cofounded Matrix Semiconductor (acquired by Sandisk in 2006). He is the founder of ZeroG Wireless.

10:00–10:25 AM — Break

1. RF & mmWave VCOsTuesday 10:25 AM — *TRAVIS I & II*

Session Chair: L. Van den Oever

Co-Chair: J. Rogers

(1.1) 10:25–10:50 AM – A 125 GHz LC-VCO in a SiGe:C technology dedicated to mmW applications*R. Toupé, Y. Deval, J.-B. Bégueret*

This paper presents a 125GHz LC-VCO dedicated to mmW applications. It has been designed, within the framework of the European project DOTFIVE, with a new B3T bipolar technology developed by STMicroelectronics, in which NPN transistors reach a f_i and f_{max} of 260GHz and 340GHz respectively. Under a nominal power supply of 1.8V, the 125GHz VCO dissipates 54mA (with output buffers) for a measured phase noise of -75dBc/Hz at 1MHz offset from the 125GHz carrier and achieves a tuning range of 2GHz with a size of 0.25 mm^2 .

(1.2) 10:50–11:15 AM – A 25 GHz Wide-tuning VCO RFIC Implemented in 0.13 μm SiGe BiCMOS Technology (Student)*V. Kakani, Y. Jin, F. F. Dai*

This paper presents the design and measurement of an integrated millimeter wave wideband voltage controlled oscillator (VCO). This VCO employs the on chip transmission lines and hyperabrupt junction varactors to form high Q resonator. The VCO RFIC was implemented in a $0.13\mu\text{m}$ 200GHz ft SiGe hetero-junction bipolar transistor (HBT) BiCMOS technology. The VCO oscillation frequency is around 25GHz, targeting at the ultra wideband (UWB) and short range radar applications. The VCO phase noise was measured around -82.5dBc/Hz at 500 KHz frequency offset. It has a wide tuning range from 23.8GHz to 26.3GHz. The core of VCO circuit consumes 10mA current from a 2.2V power supply and occupies $0.56 \times 0.205\text{mm}^2$ area.

(1.3) 11:15–11:40 AM – Frequency- and Amplitude-Tunable X-to-Ku Band SiGe Ring Oscillators for Multiband BIST Applications (Student)*S. Shankar, S. Horst, J. D. Cressler*

An 8-17 GHz SiGe ring oscillator covering the X- and Ku-band for Built-in-Self-Test of multiband system-on-chip solutions is demonstrated. The oscillator features highly linear frequency control over the bandwidth, with 72% tuning range in a small form factor of 0.652 mm^2 . To the author's knowledge, this is the widest tuning range/smallest form factor combination achieved by a ring oscillator that spans both X and Ku bands. A second ring oscillator with band selectivity and output power control is also presented, covering the 9-11 GHz and 17-21 GHz bands. This oscillator features an ultra-small form factor of only 0.036 mm^2 . Both oscillator designs are based on a 3.3 V supply and were implemented in a commercially-available 180 nm SiGe platform.

(1.4) 11:40–12:05 PM – A comparison of npn vs. pnp SiGe HBT oscillator phase noise performance in a complementary SiGe platform (student)*S. Horst, P. Chakraborty, P. Saha, J. D. Cressler, H. Gustat, B. Heinemann, G. G. Fischer, D. Knoll, B. Tillack*

A comparison of cross-coupled oscillator performance is presented for a high-speed, complementary SiGe (C-SiGe = *npn* + *pnp*) BiCMOS

platform with matched *nnp* and *pnnp* performance. Results show with all factors held constant, the *pnnp*-only VCO design holds an advantage in white FM phase noise over its *nnp* counterpart at constant current. The reduced noise in the *pnnp*-only VCO is shown to stem from the device's reduced β compared to the *nnp*, which reduces conversion of the thermal noise associated with the base resistance to the output node. The phase noise reduction occurs in a region that reduces the white FM noise of the oscillator, which can have advantages in PLL design.

(1.5) 12:05–12:30 PM – Fully-Integrated 1-Dimensional RF Coupled-Oscillator Network for Phase-Shifterless Phased Array Systems (Student)

J. Lopez, D. Y. C. Lie, B. K. Meadows, J. Cothorn

A fully-monolithic 3-element array of coupled voltage-controlled-oscillator (VCO) network was fabricated in a 0.18 μ m SiGe BiCMOS process for potential use in a Rx/Tx modules. A digitally controlled on-chip passive network was designed and used for controlling the coupling strength across the array VCO units. The operational bandwidth of this core network resides in the S-Band from 1.2GHz to 1.7GHz. The integrated VCO network can be injection-locked via an external RF source to achieve excellent phase noise performance. These characteristics make this coupled-VCO network a very attractive choice for possible use in phased-array radar applications. The chip's total power consumption is 30mW (12mA at 2.5V).

2. High Bitrate Circuits

Tuesday 10:25 AM – **TRAVIS III**

Session Chair: B. Hecht

Co-chair: H. Veenstra

(2.1) 10:25–11:15 AM – Burst-mode Optical Receiver ICs for Broadband Access Networks (Invited)

M. Nakamura, S. Nishihara, T. Ito, T. Kurosaki, M. Nogawa, Y. Ohtomo

This paper provides an overview of burst-mode optical receiver ICs for broadband access networks. A passive optical network (PON) system is a cost-effective broadband access system whose use has been spreading worldwide. A key device in such a system is an optical receiver IC with a quick response and high sensitivity that realizes high efficiency in data transmission. This paper also reports burst-mode optical receiver ICs fabricated using 0.25- μ m SiGe BiCMOS technologies for a 10G-EPON system, which is a promising access network for a next generation PON system. It features fast gain and offset controls for burst-mode operation. The results show that SiGe BiCMOS can provide high performance and cost-effective receiver ICs for 10G-class PON systems.

(2.2) 11:15–11:40 AM – Static Frequency Dividers up to 125GHz in SiGe:C Bipolar Technology

H. Knapp, T. F. Meister, W. Liebl, D. Claeys, T. Popp, K. Aufinger, H. Schäfer, J. Böck, S. Boguth, and R. Lachner

This paper presents CML and ECL static frequency dividers in a SiGe:C bipolar process with a cut-off frequency f_T of 225 GHz. Speed/power trade-offs are investigated by comparing three different circuit versions. Each contains two master-slave flip-flops to achieve a divide ratio of four. The first version uses current-mode logic flip-flops and achieves a maximum operating frequency of 78 GHz at a power

consumption of only 13mW in the first flip-flop. Two versions use emitter-coupled logic with one and two emitter follower stages in the feedback path, respectively. The low-power divider with one emitter follower operates up to 99 GHz while the second circuit achieves a maximum operating frequency of 125 GHz. The power consumption in the first flip-flop is 62mW and 232mW, respectively. The circuits use standard flip-flops without speed-enhancement techniques, such as split load resistors, inductive peaking, or asymmetric latches.

(2.3) 11:40–12:05 PM – Fully Differential, 40Gb/s Regulated Cascode Transimpedance Amplifier in 0.13 μm SiGe BiCMOS Technology (Student)

S. B. Amid, C. Plett, P. Schvan

A broadband differential Transimpedance Amplifier (TIA) has been designed and measured in 0.13 μm BiCMOS Technology. Regulated Cascode (RGC) configuration has been employed to reduce the effect of the large parasitic capacitor of the PIN diode. The C_{PD} is assumed to be 300fF. The TIA has 53dBQ differential transimpedance gain and 28GHz measured bandwidth. The total simulated differential input referred noise is 3.1 μA up to 34GHz. The TIA chip including the TIA and 3 stages of buffer consumes 110mW power from a 3V power supply. The active chip area is 330 μm ×210 μm and the total chip area including pads is 1050 μm ×530 μm .

3. BiCMOS, C-BiCMOS, C-Bipolar Technologies and Devices

Tuesday 10:25 AM — LAKEVIEW

Session Chair: J. John

Co-Chair: J. van Huynenbroeck

(3.1) 10:25–10:50 AM – A High Performance 36V Complementary Bipolar Technology on Low Thermal Resistance Compound Buried Layer SOI Substrates

S. J. Harrington, A. Bousquet, S. Nigrin, S. Suder, B. M. Armstrong

In this paper a new high voltage, high performance, high packing density, silicon complementary bipolar technology on novel low thermal resistance compound buried layer (CBL) SOI is reported. NPN and Vertical PNP devices have been fabricated with matched DC and AC characteristics, cutoff frequencies of 3 GHz and breakdowns greater than 36 Volts. The thermal resistance of the fabricated devices confirms the superior performance of the CBL SOI substrates.

(3.2) 10:50–11:15 AM – CBC8 A 0.25 μm SiGe-CBiCMOS Technology Platform on Thick-Film SOI for High-Performance Analog and RF IC Design

J. A. Babcock, G. Cestra, W. van Noort, P. Allard, S. Ruby, J. Tao, R. Malone, A. Buchholz, N. Lavrovskaya, W. Yindeepol, C. Printy, J. Ramdani, A. Labonte, H. McCulloh, Y. Leng, P. McCarthy, D. Getchell, A. Sehgal, T. Krakowski, S. Desai, C. Joyce, P. Hojabri, and S. Decoutere

A production released complementary-SiGe BiCMOS technology on SOI has been developed for high speed analog and RFIC applications. It features matched SiGe:C PNP and NPN transistors. The PNP shows cutting edge performance metrics with $\beta \cdot V_A = 17,000$ and near record $f_T \cdot BV_{CEO} \geq 195\text{GHz} \cdot \text{V}$ for a 5V process while demonstrating best in

class linearity on a fully differential amplifier design. A modular process flow was leveraged to enhance the Analog design needs for the platform. For higher-speed lower power, we also demonstrate a low voltage SiGe NPN with peak f_T of 50 GHz at low-bias ($V_{CE} = 0.5V$), ideal for load line drive. Finally, we discuss core CMOS devices which utilize a dual-gate oxide process for improved mixed-signal mixed-voltage design and better optimization of digital blocks.

(3.3) 11:15–11:40 AM – A High Performance, Low Complexity 14V Complementary BiCMOS Process Built on Bulk Silicon

T. Thibeault, E. Preisler, J. Zheng, L. Lao, P. Hurwitz, M. Racanelli

This paper details a new 14V Complementary BiCMOS (CBiCMOS) addition to the TowerJazz SBC35 family of BiCMOS technologies that previously supported BV_{ceo} values up to 6V. The bipolar architecture is nearly identical with that used in the lower voltage technologies. The complementary bipolar transistors are paired with 5V CMOS currently available in our SBC35 family. This technology offers high RF performance 14V NPN transistors and PNP transistors with low process complexity. The paper describes a simplified process flow and a demonstration of the key device performance metrics.

(3.4) 11:40–12:05 PM – Vertical Profile Optimization for +400GHz f_{MAX} Si/SiGe:C HBTs (Student)

T. Lacave, P. Chevalier, Y. Campidelli, M. Buczko, L. Depoyan, L. Berthier, G. Avenier, C. Gaquière, A. Chantre

This paper summarizes the work carried out on the vertical profile of double-polysilicon SiGe:C HBTs to get f_{MAX} above 400 GHz. The effects of the final spike annealing temperature, the emitter doping species, the base and collector doping levels and the Si capping layer thickness are presented and discussed.

(3.5) 12:05–12:30 PM – Layout and Spacer Optimization for High-Frequency Low-Noise Performance in HBT's

T. Vanhoucke, J.J.T.M. Donkers, G.A.M Hurkx, P.H.C. Magnée, R. van Dalen, J. H. Egbers D.B.M. Klaassen

In this work we study improvements of the high-frequency noise performance of HBT devices by means of layout and spacer optimization. Using an equivalent circuit, we identify the dominant noise sources and demonstrate that the reduction of the base resistance induced thermal noise by means of dotted emitters in combination with lowering the edge contribution of the base-emitter capacitance (e.g. by emitter-base spacer optimization) translates into higher noise performance.

Lunch Break

12:30–2:00 PM

4. mmWave TransceiversTuesday 2:00 PM – *TRAVIS I & II*

Session Chair: A. Wang

Co-Chair: W. van Noort

(4.1) 2:00–2:25 PM – A Fully Integrated Q-band Bidirectional Transceiver in 0.12-um SiGe BiCMOS Technology*J. Kim and J. F. Buckwalter*

A fully integrated Q-band (40–45 GHz) bidirectional transceiver is demonstrated in a 0.12- μm SiGe BiCMOS technology. The RF front-end design eliminates the need for transmit/receive switches by demonstrating a novel PA/LNA circuit. The transceiver has a transmit conversion gain of 35 dB with a 3-dB bandwidth of 4 GHz. The $\text{OP}_{1\text{dB}}$ is 8.5 dBm and P_{sat} is 9.5 dBm. The transceiver has a receive conversion gain of 34 dB with a 3-dB bandwidth of 3 GHz. The noise figure is 4.7 dB and $\text{OP}_{1\text{dB}}$ is -5 dBm at 43 GHz. The chip consumes 119.4 mW when transmitting and 54 mW when receiving, and overall chip size is 1.6 mm \times 0.8 mm including pads. To the authors' knowledge, this work represents the first switchless millimeter wave bidirectional transceiver in a CMOS or BiCMOS processes.

(4.2) 2:25–2:50 PM – A High-Linearity Inverse-Mode SiGe BiCMOS RF Switch (Student)*A. Madan, J. Cressler, and A. Joseph*

The utilization of inverse-mode operation of the SiGe HBT in a single-pole, single-throw RF switch designed for high-linearity and high-power handling applications is investigated for the first time. By swapping the base-emitter junction with base-collector junction for switching, record linearity performance is obtained for SiGe BiCMOS switches at X-band frequencies, while maintaining comparable insertion loss. An IIP3 of 35 dBm and P1dB of 20 dBm is obtained while consuming 29.7 mW of *dc* power in the ON state. The inverse-mode switch did not show any degradation up to an RF power level of 30 dBm. The reliability mechanisms in SiGe BiCMOS RF switches is understood to be junction damage in the series-diode switching element.

(4.3) 2:50–3:15 PM – A fully integrated 77-GHz Radar Transmitter based on a Low Phase-Noise 19.25-GHz Fundamental VCO*F. Starzer, A. Fischer, H. P. Forstner, H. Knapp, F. Wiesinger, A. Stelzer*

A 77-GHz automotive radar transmitter is presented. The transmitter is based on a 19.25-GHz Colpitts voltage controlled oscillator, that feeds two cascaded frequency doubler stages. In a following medium power amplifier (MPA) the signal recovers after frequency transformation. Finally a power amplifier (PA) adds 6 dB to the power level after the MPA. In addition, an emitter follower stage connected to the oscillators output drives a switchable divide-by-16/32 stage realized in emitter-coupled-logic (ECL).

(4.4) 3:15–3:40 PM – Investigation and Reduction of Frequency Pulling in SiGe mm-Wave VCOs at Limited Power Consumption*N. Pohl, H.-M. Rein, T. Musch, K. Aufinger, J. Hausner*

The influence of load variation on the oscillation frequency of wideband mm-wave VCOs in a SiGe bipolar technology is investigated theoretically and experimentally. This load variation can change the

real part of the voltage gain of the oscillating transistor stage, which varies the input impedance of this stage via C_{CB} , thus leading to the so called *frequency pulling* Δf_{osc} . This effect can be reduced, at relatively low power dissipation (240mW in total), by use of a common-base stage at the output of the oscillator and, furthermore, by two cross-coupled compensation diodes in the oscillator core. The latter measure slightly reduces the tuning range (from $\Delta f_{osc} = 24.5\text{GHz}$ to still reasonable $\Delta f_{osc} = 18.7\text{GHz}$), without degrading phase noise and output power (-97 dBc/Hz at 1MHz offset frequency and 11 dBm at center frequency, respectively).

(4.5) 3:40–4:05 PM – A 77-GHz SiGe Frequency Multiplier (x18) for Radar Transceivers

A. Fischer, F. Starzer, H.-P. Forstner, E. Kolmhofer, A. Stelzer
For 77-GHz automotive radar applications, a monolithic frequency multiplier with a multiplication factor of 18 is presented. The main circuit of the multiplier chain consists of two frequency tripler and one doubler. Additionally interstage amplifiers and filters are integrated in a 200-GHz SiGe:C production technology. The output power is -1dBm for a wide input power range (-20dBm to +8 dBm) at room temperature and 76.5 GHz output frequency. The output power flatness is better than 2 dB for an output frequency range of 69 GHz to 80 GHz. The power consumption of the multiplier is 170mW at a single supply voltage of 3.3V.

5. Integrated BiCMOS Components

Tuesday 2:00 PM – *TRAVIS III*

Session Chair: J. Donkers

Co-Chair: G. Avenier

(5.1) 2:00–2:50 PM – Silicon Integrated Photoreceivers (Invited)

W.-Y. Choi, M.-J. Lee, J.-S. Youn

Integrated photoreceivers having photodetectors and necessary electronic circuits on the same chip are an essential element of high-performance optical interconnects. Various techniques for realizing integrated photoreceivers with the standard CMOS and BiCMOS technologies are reviewed.

(5.2) 2:50–3:15 PM – Hyperabrupt-Junction Varactor for mmWave SiGe:C BiCMOS, Enabling 77GHz VCO/TX with 13-15GHz Tuning Range

V. P. Trivedi, J. Kirchgessner, J. P. John, P. Welch, D. Morgan, S. Stewart, R. Peterman, D. Hammock, J. Nivison, O. Hartin, S. Shams, I.-S. Lim, H. Li, S. Trotta, D. Salle, W. M. Huang

A millimeter-wave hyperabruptjunction varactor (HAVAR) enabling 77GHz VCO/TX with 13-15GHz tuning range and better than -70dBc/Hz phase noise at 100kHz offset has been integrated in SiGe:C BiCMOS for automotive radar products. The HAVAR predominantly uses existing processes for low-cost integration and minimal process complexity. Optimization of TR-Q through HAVAR width allows TR up to 2.7 and Q_{min} up to 10.

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(5.3) 3:15–3:40 PM – Design and Optimization of Silicon JFET in 180nm RF/BiCMOS Technology

Y. Shi, R. M. Rassel, R. A. Phelps, B. Rainey, J. Dunn, D. Harame

In this paper, we discuss a method to extrapolate intrinsic and extrinsic R_{on} component for a JFET. The results provide the guideline to lower R_{on} , hence to achieve competitive “ R_{on} vs. pinch off (V_{off})” benchmark. The impacts on channel scaling and process variation are discussed. Besides, an improved RESURF condition is achieved using one of the experimental splits. The optimized JFET is demonstrated with 50% lower R_{on} , while maintaining low V_{off} , and BV_{dss} of 11 V.

(5.4) 3:40–4:05 PM – Integrated Si-LDMOS Transistors for 11 GHz X-Band Power Amplifier Applications

R. Sorge, A. Fischer, A. Mai, P. Schley, J. Schmidt, Ch. Wipf, R. Pliquett and R. Barth

The integration of RF NLD MOS transistors into a 0.13 μm CMOS process for operating at X-Band (8.5-10.5 GHz) frequencies with over 11 dB gain and 0.25 W/mm power density and 22% power added efficiency at 1 dB output power compression is presented. The self aligned NLD MOS was modularly integrated into IHP's 130 nm SiGe BiCMOS platform targeting 1 W X-Band power amplifiers for radar and satellite communication applications.

6. State-of-the-Art Modeling and Characterization

Tuesday 2:00 PM — **LAKEVIEW**

Session Chair: D. Weiser

Co-Chair: B. Ardouin

(6.1) 2:00–2:25 PM – Large-signal Modeling of SiGe HBT for PA Applications

T.-Y. Lee, S. Lee, P. Zampardi, J. Kang

Accurate modeling of large-signal behavior of power amplifiers (PAs) is key in minimizing the number of design spins and design cycle time. This paper presents the 1- and 2-tone large-signal behavior of SiGe HBT as a function of input power, frequency, bias, and transistor geometry. While the transistor's weak non-linearity is largely determined by the trans-conductance (G_m) and the quasi-static (QS) charge-storage of the transistor, its high-power large-signal behavior heavily depends on the high-current gain roll-off characteristics and supply clamping. It is discussed from a PA-design standpoint how the SiGe bandgap engineering impacts the large-signal behavior through steeper gain compression at high currents and high power. Finally an accurate prediction of critical parameters of a practical WCDMA PA was demonstrated with careful accounting of the high-current effects in the SiGe HBT transistor.

(6.2) 2:25–2:50 PM – Application of On-Wafer Calibration Techniques for Advanced High-Speed BiCMOS Technology

A. Rumiantsev, P. Sakalas, F. Pourchon, P. Chevalier, N. Derrier, M. Schröter

On-wafer RF calibration methods are compared to the conventional Impedance Standard Substrate (ISS) calibration combined with

dummies de-embedding approach for transistors of an advanced BiCMOS process. We discuss the design of Silicon customized calibration standards, addressing specifics of the silicon BiCMOS process. Our results show that on-wafer calibration methods, such as multiline TRL or LRM+, are the most suitable approaches for accurate characterization of sub-THz SiGe HBT's.

(6.3) 2:50–3:15 PM – On-wafer Passives De-Embedding Based on Open-pad and Transmission Line measurement

A. Hamidipour, M. Jahn, F. Starzer, X. Wang, A. Stelzer

In this paper, a new de-embedding technique based on open-pad and Transmission Line (TL) measurement is discussed. This technique can be used as an efficient approach to characterize on-chip passives in the millimeter wave range. Using open-pad measurement, parallel parasitics are extracted and removed in the first step. Cross-talk parasitics between two pads that are kept at a constant distance can be assumed constant, and thus both cross-talk and parallel parasitics can be removed. Subsequently, the transfer function matrix of a single-ended TL is used to de-embed series parasitics from the measurement results. This calculation leads to a better extraction and removal of the series parasitics compared to using a conventional short dummy pattern. The measurement results are in a close agreement with the simulations up to 110 GHz.

(6.4) 3:15–4:05 PM – Is SPICE Good Enough for Tomorrow's Analog? (Invited)

L. Nagel, C. McAndrew

SPICE is nearly 40 years old and has played an important part in the design of thousands of circuits, both integrated and discrete. While the size and complexity of integrated circuits has increased exponentially over the lifetime of SPICE, reports of the obsolescence of SPICE are greatly exaggerated. This paper describes the evolutionary changes in SPICE and the underlying compact models employed by SPICE that will be required to continue the design of analog integrated circuits for the next forty years.

4:05–4:25 PM — Break

7. 4G Radio Design and Power Amplifiers

Tuesday 4:25 PM – *TRAVIS I & II*

Session Chair: D. Teeter

Co-Chair: G. Hau

(7.1) 4:25–5:15 PM – 4th Generation Wireless Transceiver Design (Invited)

L. Larson, P. Asbeck and D. Kimball

4th generation wireless systems will require even higher levels of integration, wider bandwidths and innovative strategies to manage the growing number of available frequency bands. This paper will summarize some of the key circuit and system design approaches for 4th generation wireless transceivers.

(7.2) 5:15–5:40 PM – A Highly Efficient SiGe Differential Power Amplifier Using An Envelope-Tracking Technique for 3GPP LTE Applications (Student)

Y. Li, J. Lopez, D. Y. C. Lie, K. Chen, S. Wu, T.-Y. Yang

This paper presents a highly-efficient polar transmitter (TX) system that adopts the envelopetacking (ET) technique with a differential SiGe power amplifier (PA) for 3GPP Long Term Evolution (LTE) applications. The differential PA was designed using a cascode topology, reaching power-added efficiency (PAE) of 50% at output power of 22dBm in continuous wave (CW) mode. The experimental data also shows that the proposed ET-based polar TX system with the cascode PA delivers 21dBm average output power with 33.6% PAE at 1.42 GHz, while also meeting the LTE 16QAM linearity specs for both error vector magnitude (EVM) and TX emission mask without the need of PA predistortion.

(7.3) 5:40–6:05 PM – A 91 to 110-GHz Tapered Constructive Wave Power Amplifier in a 0.12 μ m SiGe BiCMOS Process

N. Kalantari, J. F. Buckwalter

A W-band, tapered constructive wave power amplifier (TCWPA) has been designed and fabricated in a 0.12 μ m SiGe BiCMOS technology. The amplifier has a 3 dB BW of 19 GHz from 91-110 GHz and a maximum gain of 12.5 dB at 101 GHz. At 98 GHz, OP_{1dB} is 4.9 dBm. At 97 GHz, P_{sat} is 5.9 dBm and the PAE is 7.2%. The amplifier operates from a 2.4 Vsupply and occupies an area of 0.22 mm².

(7.4) 6:05–6:30 PM – Millimeter-wave Beamforming Circuits in SiGe BiCMOS

M. Elkhoully, C.-S. Choi, S. Glisic, C. Scheytt, F. Ellinger

Integrated millimeter-wave 2 bit and 3 bit phase shifters and 4 channel beamforming network are presented in this paper. The 2 bit phase shifter exhibits 4° RMS phase error and a RMS gain error < 1 dB. In the 55-67 GHz range, the 3 bit phase shifter shows RMS phase error < 7° and a RMS gain error < 1 dB. The 4 channel beamforming network consists of four 2 bit RF phase shifter and a fully differential passive power distribution network. Between the 4 channels, the beamforming network exhibits less than 4° and 0.6 dB RMS phase and amplitude mismatch, respectively. The beamforming chip and the phase shifters are fabricated in SiGe BiCMOS technology. The 2 bit and 3 bit phase shifters draw 7 mA and 10 mA respectively from a 3.3V supply. The circuits are well suited for highly integrated beamforming millimeter-wave transceivers.

8. Robustness and Thermal Limitations

Tuesday 4:25 PM – **TRAVIS III**

Session Chair: L. Nanver

Co-Chair: J. Prasad

(8.1) 4:25–4:50 PM – A Large-signal RF Reliability Study of Complementary SiGe HBTs on SOI Intended for Use in Wireless Applications (Student)

S. Seth, T. Thrivikraman, P. Cheng, J. D. Cressler, J. A. Babcock, A. Buchholz

For the first time, a large-signal RF stress study of complementary (*nnp* + *pnnp*) SiGe HBTs on thick-film SOI is performed, and analyses based on device physics are presented, shedding light on the

observed failure mechanisms of these C-SiGe HBTs at very high RF input power. Two types of *nnp* SiGe HBTs, low-breakdown voltage (LVNPN) and high-breakdown voltage (HVNPN) devices, as well as a high-breakdown voltage *pnnp* SiGe HBT (HVPNP) in a 250 nm C-SiGe on SOI process are investigated. It is shown that the HVPNP can withstand aggressive RF stress for longer periods of time, compared with the LVNPN and the HVNPN, which succumb to several interesting modes of catastrophic device failure. A case is made for the use of *pnnp* SiGe HBTs in sensitive RF front-ends that may be exposed to non-limited high RF power due to leakages in the transmit/receive (T/R) path or RF reflections.

(8.2) 4:50–5:15 PM – Impact of layout and technology parameters on the thermal resistance of SiGe:C HBTs

V. d’Alessandro, I. Marano, S. Russo, D. Céji, A. Chantre, P. Chevalier, F. Pourchon, N. Rinaldi

Calibrated 3-D numerical simulations supported by DC experimental data are employed to quantify the impact of the key layout and technology parameters on the thermal resistance of 300 GHz SiGe heterojunction bipolar transistors (HBTs) so as to define proper optimization criteria. The geometry parameters of a simple scalable model are optimized to describe the thermal resistance dependence upon emitter dimensions for the HBTs under analysis.

(8.3) 5:15–5:40 PM – An Investigation of Electro-thermal Instabilities in 150 GHz SiGe HBTs Fabricated on SOI (Student)

P. S. Chakraborty, S. J. Horst, K. A. Moen, M. Bellini, J. D. Cressler

We investigate, for the first time, the electro-thermal stability of 150 GHz SiGe HBTs that were optimized for bulk-Si and then fabricated on SOI substrates to enable a direct comparison. AC, DC and pulsed measurements are used to characterize the devices and study the onset of electro-thermal instabilities. Implications of electro-thermal feedback induced instabilities resulting from self-heating are discussed, along with consequent electrical biasing constraints imposed on the device. Figures-of-merit are proposed as effective tools for comparing devices with strong self-heating effects. TCAD is used to predict the implications for performance scaling and BiCMOS technology development for SiGe on SOI platforms.

(8.4) 5:40–6:05 PM – Temperature Interaction of Early Voltage, Current Gain and Breakdown Characteristics of npn and pnp SiGe HBTs on SOI

J. A. Babcock, L. J. Choi, A. Sadovnikov, W. van Noort, C. Estonilo, P. Allard, S. Ruby, G. Cestra

We present a comprehensive investigation of temperature dependence of breakdown voltage, DC current gain (β), and Early voltage (V_A) for complementary SiGe-*nnp* and SiGe-*pnnp* bipolar transistors fabricated on an advanced CBiCMOS technology on thick-film SOI. Both SiGe-*nnp* and SiGe-*pnnp* transistors show decreasing V_A as ambient operating temperature increases from -60°C to $+200^\circ\text{C}$ for low collector current densities ($J_C \leq 5.0 \mu\text{A}/\mu\text{m}^2$) with a near linear inverse temperature ($1/T$) relationship. We also demonstrate in the region historically defined by weak self-heating interactions that V_A maintains minimal sensitivity to ambient operating temperature.

(8.5) 6:05–6:30 PM – Design Optimization of Adjustable Triggering Dual-Polarity ESD Protection Structures (Student)

J. Liu, L. Lin, X. Wang, Z. Shi, S. Fan, H. Tang, A. Wang, Y. Cheng

We report design optimization of new lowtriggering dual-directional SCR (LTdSCR) ESD protection structures in BiCMOS. Design optimization techniques to adjust ESD triggering voltage (V_{t1}), as well as its impacts on ESD holding voltage (V_h) and ESD protection capability, are discussed. Measurements show very low and adjustable V_{t1} , low leakage (I_{leak}), low noise figure (NF), low ESD-induced parasitic capacitance (C_{ESD}) and fast ESD triggering time (t_i). High ESD protection to Si ratio of $ESDV \sim 7.49V/\mu m^2$ is achieved.

9. High-Frequency and Noise Modeling

Wednesday 4:25 PM – **LAKEVIEW**

Session Chair: P. Tounsi

Co-Chair: R. Malladi

(9.1) 4:25–4:50 PM – BJT Small-Signal Equivalent Circuit Representation

C. C. McAndrew, L. Nagel

This paper presents a small-signal equivalent circuit for bipolar transistors that is a rigorously derived from linearization of the large-signal model. The model includes additional capacitance and transcapacitance elements compared to the common hybrid- π model.

(9.2) 4:50–5:15 PM – An Investigation of Collector-Base Transport in SiGe HBTs Designed for Half-Terahertz Speeds (Student)

J. Yuan, J. D. Cressler, K. A. Moen, P. S. Chakraborty

A new method is introduced to investigate electron transport in the collector-base space charge region of SiGe HBTs designed for half-Terahertz speeds. Using commercially-available Monte Carlo and hydrodynamic TCAD tools, one can eliminate the fundamental limitations of hydrodynamic models related to velocity overshoot and impact ionization. The method is verified in a 200-GHz SiGe technology and then applied to hypothetical 350-GHz and half-THz (500 GHz) SiGe HBTs. This new approach requires far less computational complexity than classical Monte Carlo tools.

(9.3) 5:15–5:40 PM – Base Resistance Distribution in Bipolar Transistors: Relevance to Compact Noise Modeling and Extraction from Admittance Parameters (Student)

F. Vitale, R. Pijper, R. van der Toorn

We discuss the relevance of the distribution of the base resistance of planar bipolar transistors with respect to noise and small-signal characteristics. We present analytical results for admittance parameters in terms of elements of the small-signal equivalent circuit of the Mextram compact model and discuss extraction of base resistance distribution parameters from measured admittance parameters for selected cases.

(9.4) 5:40–6:05 PM – An Investigation of Low-Frequency Noise in Complementary SiGe HBTs on SOI (student)

P. Cheng, S. Horst, S. Phillips, S. Seth, R. Mills, J. D. Cressler, G. Cestra, T. Krakowski, J. A. Babcock, A. Buchholz

Low-frequency noise in complementary SiGe HBTs on SOI is investigated. S_{ib} is extracted using a custom measurement setup, and the corresponding K factors are compared across multiple SiGe technology platforms for better understanding of SiGe evolutionary trends. We find that low-frequency noise has generally decreased with scaling for both *nnp* and *pnp* SiGe HBTs, despite the low thermal cycles that aggressive scaling techniques utilized. In general, *pnp* SiGe HBTs have higher noise than *nnp*'s, and this is true for Si BJTs as well as SiGe HBTs. The SiGe HBTs on SOI from a new C-SiGe platform presented here fit these trends, demonstrating their maturity and competitiveness. Low input impedance noise measurement were also measured and analyzed in these SiGe HBTs, using a common-collector and a common-base configuration. We find that noise term S_{ic} can be significant at high injection levels.

(9.5) 6:05–6:30 PM – Noise modeling of advanced technology high speed SiGe HBTs

P. Sakalas, J. Herricht, M. Ramonas, M. Schroter

Noise parameters of SiGe HBTs fabricated in different technologies were measured in the 1-26 GHz frequency range. The standard dc, ac characteristics and noise parameters were compared to the compact model HICUM. Very good agreement was obtained for all technologies. The noise parameters were simulated with a new noise correlation model. A sophisticated noise model implementation, based on system theory was realized in Verilog-A. The model was further verified up to 500 GHz against TCAD simulations. The compact realization of the new noise correlation model is applicable to all SPICE-like circuit simulators.

6:30–7:00 PM Break

7:00–11:00 PM Dinner Banquet

POOLSIDE TEXAS BBQ

Wednesday, October 6, 2010

10. Emerging Technologies

Wednesday 8:00 AM – *TRAVIS BALLROOM, I, II, III*

Session Chair: D. Lie

8:00–8:15 AM — Session Welcome and Introduction

D. Lie

(10.1) 8:15–8:55 AM — Graphene for Electronic Applications – Transistors and More (Invited)

F. Schwierz, Technical University Ilmenau, Germany

During the last five years, the new material graphene has gained increasing attention in the device community. The progress in the development of graphene transistors is breathtaking and graphene-based devices are now considered as an option for a post-Si electronics. However, to realistically assess the potential of graphene, the existing problems with graphene and the options to solve them have to be analyzed carefully. The present paper provides an overview of the current status of graphene transistor development and discusses the prospects and problems of these devices.

(10.2) 8:55–9:35 AM — Antennas on Silicon for Millimeterwave Applications – Status and Trends (Invited)

Ch. Person, Lab-STICC/Telecom Bretagne, France

We discuss in this paper about the recent development of Antennas on Chip (AoC), especially in the context of emerging applications in the millimetre wave frequency range, like WLAN @ 60Ghz, automotive radars (76-81GHz) as well as imaging system (94Ghz). Limitations due to the specific environment of such antennas integrated on Silicon are described and analysed first. Then, we focus on the different approaches which can be investigated for enhancing the performances of such highly integrated radiating modules, especially dedicated to future SiP (System in Package) and SoC (System on Chip) chips for RF Microelectronics.

(10.3) 9:35–10:15 AM — The Future of Medical Electronics (Invited)

K. Vansath, Texas Instruments, USA

Medical electronics have a very important role to play in improving the quality of health care in the form of diagnosis and therapy of illness. In addition, they have an equally important role in the prevention of sickness. The success of such devices depends on the ability to measure and interpret the wide variety of signals linked to the underlying physical condition. For example, in ultrasound systems, the electronics needs to be able to analyze signal strength varying over 100dB in magnitude. This talk will cover the range of process and design requirements to meet these requirements. Future trends and directions will also be discussed.

10:15–10:35 AM — Break

11. Mixers and LNAsWednesday 10:35 AM – *TRAVIS I & II*

Session Chair: D. Lie

Co-Chair: F. Fa Dai

(11.1) 10:35–11:00 AM – A SiGe:C BiCMOS LNA for 94GHz band applications (Student)*R. R. Severino, T. Taris, Y. Deval, D. Belot, J. B. Begueret*

A new low noise amplifier (LNA) dedicated to 94GHz band has been implemented in a 130nm BiCMOS technology intended for millimeter waves applications. The circuit is a single stage cascode amplifier utilizing transmission lines and MIM capacitors for input, output and inter-stage matching. On chip measurements show a 9.08dB maximum peak of power gain at 94.7GHz and a 1dB compression point at -14.9dBm of input power. The noise figure is 8.6dB and the power consumption is 13mW.

(11.2) 11:00–11:25 AM – A Low-Power 60GHz Receiver Front-End with a Variable Gain LNA in SiGe BiCMOS Technology*Y. Sun and C. J. Scheytt*

This paper presents a fully differential low-power 60 GHz Front-End, which comprises a variable gain differential LNA and a low-power Gilbert mixer. The differential LNA features a current folded architecture to save power consumption. Its gain can be tuned from zero to 17.3 dB. It is 15.3 dB for fully differential operation at 10 mW DC power. The measured 3 dB bandwidth is from 57 to 64 GHz. Both input and output return losses are measured to be below -10 dB in the same frequency range. The mixer core is a Gilbert cell, which consumes 1.44 mA from 3.3 V DC supply. Its voltage conversion gain is optimized to be 10 dB. This front-end is best suited for 60 GHz beam steering system where multiple front-ends are required.

(11.3) 11:25–11:50 AM – A Tunable, SiGe X-band Image Reject Mixer (Student)*P. K. Saha, J. D. Cressler*

A SiGe 8-12 GHz image reject mixer with tunable performance is presented. Control voltages and currents allow the mixer performance to be "healed", nullifying effects of process variation or environmental changes. Conversion gain greater than 10 dB and output P1dB greater than 0 dBm were obtained in measurement. An image rejection ratio (IRR) of greater than 40 dB was obtained after tuning, a 25 dB improvement over pre-tuned results. The mixer was fabricated in a 150 GHz peak f_T SiGe BiCMOS process and consumes 200 mA of current operating on a 4 V rail.

(11.4) 11:50–12:15 PM – A 77-GHz Down-Conversion Mixer Architecture with Built-In Test Capability in SiGe Technology*D. Kissinger, H. Knapp, L. Maurer, R. Weigel*

A 77-GHz double-balanced mixer in a 200GHz ft silicon-germanium technology is presented. The proposed mixer architecture is capable of simultaneous direct up- and down-conversion of two separate input signals without additional power consumption. An up-converted low-frequency test signal is coupled back into the receiver RF input path to enable a built-in functionality test of the down-conversion path of the mixer. The circuit exhibits a conversion gain of 20 dB and draws 22mA from a 3.3V supply. The fabricated chip occupies an area of $1028 \times 1128 \mu\text{m}^2$.

12. New Device ConceptsWednesday 10:35 AM – *TRAVIS III*

Session Chair: J. Babcock

Co-Chair: P. Zampardi

(12.1) 10:35–11:25 AM – Design Concepts for Semiconductor based Ultra-Linear Varactor Circuits (Invited)*C. Huang, K. Buisman, L. K. Nanver, P. J. Zampardi, L. E. Larson, L. C. N. de Vreede*

For the implementation of RF tunable components, semiconductor based varactors provide advantages in terms of low control voltage, high capacitance density, low packaging costs, high reliability and technology compatibility. In this paper, an overview is given of the linearization approaches for semiconductor based ultra-linear varactors. Implementation issues regarding the optimum doping profiles are discussed. Design considerations for dedicated bias networks that provide optimum thirdorder intermodulation cancellation for the various varactor configurations are presented. To give an indication of the system-level responses for linear varactors, a varactor-based “true” time delay phase shifter is designed and the system-level linearity parameters, like adjacent channel power ratio (ACPR) and error vector magnitude (EVM), are evaluated for various application conditions.

(12.2) 11:25–11:50 AM – Collector Region Design and Optimization in Horizontal Current Bipolar Transistor (HCBT)*T. Suligoj, M. Koričić, H. Mochizuki, S. Morita, K. Shinomura, H. Imai*

Three different types of the n-collector region of Horizontal Current Bipolar Transistor (HCBT) are analyzed and compared. The optimum n-collector profile suppresses the charge sharing effect between the intrinsic and extrinsic base regions, resulting in the uniform base width and electric field in the intrinsic transistor. This implies a maximum BV_{CEO} and an optimum $f_T \cdot BV_{CEO}$ product among compared structures. The HCBT with a selectively implanted collector (SIC) is introduced and examined. It reduces R_C and increases f_T comparing to the other n-collector designs. The analyses give the guidelines for the optimum HCBT design for targeted applications.

(12.3) 11:50–12:15 PM – Modeling of a Novel NPN-SiGe-HBT Device Structure Using Strain Engineering Technology in the Collector Region*M. Al-Sa'di, S. Fregonese, C. Maneux and T. Zimmer*

The impact of utilizing silicon oxide (SiO₂) strain layer on NPN-SiGe-HBT device's electrical properties and frequency response has been studied using TCAD modeling. Simulations based on hydrodynamic (HD) model have been carried out to clarify the impact of utilizing SiO₂ strain layer in the collector region on the device performance. Simulation results show that NPN-SiGe-HBT device employing SiO₂ strain layer in the collector region exhibit better high frequency characteristics in comparison with an equivalent conventional HBT device. An approximately, 14% of improvement in f_T , and 9% of improvement in f_{MAX} have been achieved. Despite the very small decrease in the break down voltage (BV_{CEO}) value (~1%), the $f_T \cdot BV_{CEO}$ product enhancement is about 12% by means of strain engineering.

13. Analog PotpourriWednesday 10:35 AM – *LAKEVIEW*

Session Chair: H. Knapp

Co-Chair: K. Murata

(13.1) 10:35–11:00 AM – Impact of the Non-ideal Temperature Dependence of I_C - V_{BE} on Ultra-Wide Temperature Range SiGe HBT Bandgap Reference Circuits (Student)*L. Luo, G. Niu, L. Najafizadeh, J. D. Cressler*

We investigate the impact of the non-ideal temperature dependence of I_C - V_{BE} on the performance of ultra-wide temperature range SiGe HBT bandgap reference circuits. Both the slope and intercept of I_C - V_{BE} show temperature dependences that significantly differ from "ideal" Shockley theory widely used in BGR analysis and design, and are shown to have significant impact on $\Delta V_{BE}(T)$, $I_C(T)$ and $V_{BE}(T)$.

(13.2) 11:00–11:25 AM – A 5.2GHz Variable Gain Low Noise Amplifier RFIC with Adaptive Biasing for Improved Linearity (Student)*H. Xu, Y. Shi, F. F. Dai*

This paper presents a 5.2-GHz adaptively-biased variable gain- low noise amplifier (VG-LNA) using SiGe BiCMOS technology. Usage of bias and gain control simultaneously to achieve high input-referred third-order intercept point (IIP3) is demonstrated. A charge pump is used to transform the RF output signal of LNA to dc control signal. Measurement results show that with 3.3V power supply, the LNA exhibits a tunable bias from 3mA to 10.85mA with gain tuning range of 13dB, and a 14.5dBm IIP3 improvement. In the high gain mode, the noise figure of 2.82 of the LNA is achieved.

(13.3) 11:25–11:50 AM – Comparative Analysis of CML and MOS Differential Automatic Amplitude Level Control Regulators for Built-In-Self-Test Applications*B. Elkassir, S. Wane, B. Jarry, M. Campovecchio*

This paper presents a Automatic Amplitude Level Regulators (AALR) as a practical Built-In-Test (BIST) and demonstrates its application for on-chip testing and local Calibration of integrated RF blocks. The proposed circuit performs full-wave rectification and generates a dc voltage proportional to the amplitude of an RF signal over a wide frequency range. Both CML and MOS RF AALR are designed and fabricated using NXP-Semiconductors advanced BiCMOS technology process. Very low area occupation with low power consumption are demonstrated for a wide-range of RF input signal power. Digitally controlled bits are introduced scalable amplitude-level adjustment and control. Measurements show that fabricated RF test devices demonstrate detection dynamic range of 21 dB from 25 MHz to 5 GHz. Advantages and limitations of designed CML and MOS RF regulators are drawn based careful correlation analysis between simulations and measurement results.

12:15–1:30 PM — Luncheon and Luncheon Talk

Austin Ballroom

Dr. Andrew Keys

NASA-MSFC Chief Technologist

**Advanced Avionics, the Constellation Program, and
NASA's Manned Spaceflight Future**

The Advanced Avionics and Processor Systems (AAPS) project supports the National Aeronautics and Space Administration's (NASA's) Constellation program by developing avionic components, elements, and subsystems that operate within the extreme radiation and thermal environments encountered beyond low earth orbit. This talk provides a review of the development tasks within the AAPS project, including modeling of the environment and its effect on the exposed avionics, high-performance radiation-hardened processors, and low-temperature SiGe-based electronics.

***END OF MAIN BCTM
CONFERENCE***

CMRF SPECIAL SESSION: COMPACT MODELS FOR RF-MICROWAVE APPLICATIONS

**Workshop on Compact Modeling for
RF-Microwave Applications (CMRF)**

Technically Co-Sponsored by

**the IEEE Electron Devices Society & Delft Institute
for Microsystems and nano-Electronics (Dimes).**

The CMRF 2010 will explore the theme "TCAD Meets Compact Modeling". Device simulations (TCAD) and Compact Modeling (CM) are complementary. Both serve device characterization. TCAD-based physical insight may provide a basis for physics-based compact model development. TCAD and CM can be combined to predict device and even circuit performance in future technologies. Compact model parameter extraction can be supported from TCAD.

CMRF 2010 aims to bring together in a single afternoon workshop contributions from both worlds, as well as mergers of the two.

We expect presentations of industrial applications of combined TCAD and compact model-based device characterization and optimization, as well as reports from the frontiers of academic exploration and development of device simulation.

By its Workshop nature, the CMRF will provide presenters and the audience with the opportunity to reflect on experiences with TCAD and Compact Model based device characterisation, thus identifying trends and challenges in ongoing and future research. This year, a second parallel CMRF session will be devoted to modeling of thermal effects.

All BCTM registered attendees are welcome to participate in the CMRF Special Session.

**Ramses van der Toorn
CMRF Chairman 2010
TU Delft, The Netherlands**

CMRF 1. Crossing the Boundaries of ModelingWednesday 1:30 PM – *TRAVIS III*

Session Chair: R. van der Toorn

(CMRF 1.1) 1:30–2:10 PM – Large Signal RF Simulation of GaN Devices using Compact Modeling Assisted TCAD*O. Hartin**(Freescale Semiconductor)***(CMRF 1.2) 2:10–2:50 PM – Hydrodynamic Simulations for Advanced SiGe HBT's***G. Wedel, M. Schröter**(TU Dresden)***(CMRF 1.3) 2:50–3:30 PM – TCAD Assisted Reflection on Parameter Extraction for Compact Modeling***J. Steigerwald, P. Humphries**(Analog Devices)***3:30–3:45 PM — Coffee Break****CMRF 2. Crossing the Boundaries of Modeling (Continued)**Wednesday 3:45 PM – *TRAVIS III*

Session Chair: R. van der Toorn

(CMRF 2.1) 3:45–4:10 PM – Transient Voltage Overshoots of High Voltage ESD Protections Based on Bipolar Transistors in Smart Power Technology*A. Delmas, A. Gendron, M. Baffeur, N. Nolhier, C. Gill**(Freescale Semiconductor, CNRS, and Université de Toulouse)***(CMRF 2.2) 4:10–4:35 PM – Improved 2-D Regional Transit Time Analysis for Optimized Scaling of SiGe HBTs***K. Moen, J. Yuan, P. Chakraborty, M. Bellini, J. Cressler,**H. Ho, H. Yasuda, R. Wise**(Georgia Tech & Texas Instruments)*

CMRF 3. Modeling of Thermal Effects

Wednesday 3:45 PM – *TRAVIS I & II*

Session Chair: N. Rinaldi

(CMRF 3.1) 3:45–4:10 PM – Equivalent Circuit Model for Thermal Resistance of DTI Bipolar Transistors on SOI Substrate

R. Rashmi, G. A. Armstrong, S. J. Harrington, A. Bousquet, S. Nigrin

(Queen's University Belfast)

(CMRF 3.2) 4:10–4:35 PM – Dynamic Compact Thermal Model for Smart Electro-Thermal Simulation: Application to Automotive Power Device

T. Azoui, P. Tounsi, Ph. Dupuy, J-M. Dorkel

(CNRS, LAAS, Université de Toulouse, Freescale Semiconductor)

(CMRF 3.3) 4:35–5:00 PM – On the Dependence of the Thermal Resistance on Collector Properties of SiGe HBTs

F. Korndörfer

(IHP Microelectronics)

End of CMRF Special Session and of Conference

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